Q.P. Code:**16EC3801** **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester Regular & Supplementary Examinations February 2018
Digital System Design
(Common to DECS & ES)

Time: 3 hours Max. Marks:60

(Answer all Five Units 5 X 12 =60 Marks)

UNIT-I

1	a	With an example, Explain how iterative circuits are designed.	6M
	b	Explain the basic building blocks of an ASM chart	6M

OR

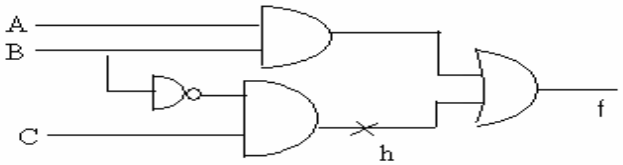
2	a	Design a circuit which generate the 2's complement of a 4-bit number using ROM	8M
	b	What are the advatages of a PAL based design of digital circuits over the ROM .	4M

UNIT-II

3	a	With a suitable example, explain Path sensitiztion method	8M
	b	Define Fault diagnosis and Bridging faults	4M

OR

4	a	Using Boolean Difference method find out the test vectors for SA0 fault on input line A and SA1 fault at line h	



8M

	b	Discuss about various types of logical faults in a digital circuits.	4M

UNIT-III

5	a	Explain Random test generation for testing digital circuits	7M
	b	With an example, explain signature analysis	5M

OR

6	a	Describe the algorithmic steps involved in PODEM.	8M
	b	With an example, explain transition count testing.	4M

UNIT-IV

7 Find the simple coloumn folding of the PLA shown below and draw the folded PLA. 12M

Coloumn	SSRs
X1	1,3
X2	2,3,6
X3	1,4,7
X4	4,5
X5	2,5
X6	2,3,6
X7	6,7

OR

8 a Conduct Homming experiment for a given machine and find out shortest Homming sequence

PS	NS,Z	
	X=0	X=1
A	A,1	E,0
B	A,0	C,0
C	B,0	D,1
D	C,1	C,0
E	C,0	D,0

6M

b Discuss about fault detection experiments. 6M

UNIT-V

9 a Write a brief note on minimal closed covers in asynchronous circuits 4M

b What is menat by hazard? Explain static and dynamic hazards. 8M

OR

10 a Write a short note on
i). Flow tables
ii). State Reduction 8M

b Explain various faults in PLA. 4M

***** END *****